

Patent Attorney's Docket No. <u>030682-103</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| In re Patent Application of |) | BOX AF |
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| Hiroyuki KAWAI et al. |) | Group Art Unit: 2124 |
| Application No.: 09/667,783 |) | Examiner: Chuong D. Ngo (7-30-0) |
| Filed: September 22, 2000 |) | Confirmation No.: 1075 |
| For: SQUARE ROOT EXTRACTION CIRCUIT AND FLOATING-POINT SQUARE ROOT EXTRACTION DEVICE |) | |

REQUEST FOR RECONSIDERATION

RECEIVED

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 DEC 1 7 2003

Technology Center 2100

Sir:

In response to the final Office Action mailed October 2, 2003, Applicants respectfully request reconsideration of the above-captioned application.

In the final rejection, the Office rejects claim 1 under 35 U.S.C. § 102(b) as allegedly being clearly anticipated by the DeTroye patent (U.S. Patent No. 4,748,581). This rejection continues to be traversed.

In the commentary accompanying the final Office Action, the Office suggests that the computation in the DeTroye patent "can be seen as being performed by only additions by the plurality of full adders (FA), and the EXOR gates (EO1) are used to provide inputs $q_i^{}q_j$ as that of the present invention to the adders." The Office also speculates that the "present specification[,] although does not disclose EXOR gates, the claimed invention as disclosed must include some logic means for providing EXOR inputs $q_i^{}q_j$ to the adders as

that of DeTroye." Applicants respectfully submit that the Office has misunderstood the reference. The DeTroye patent includes CAS (controllable add/subtract) cells in its root extraction circuit. These are disclosed at column 2, beginning at line 17, as including a full-adder circuit FA and further exclusive OR-gate E01, E02 and E03, which collectively act as a CAS cell. The confusion appears to be that the Office is extracting part of a CAS cell which includes a full adder, but not the exclusive OR-gates, and suggests therefore the circuit includes only full adders. However, Applicants respectfully submit that this circuit has to be viewed in its entirety. In its entirety, Fig. 1 discloses a CAS cell, as clearly disclosed at column 2, line 17. The mere fact that it includes a full adder as a component does not detract from the fact that it both adds and subtracts and requires four inputs a_i , b_i , c_i and p.

Furthermore, Applicants do not disclose the use of exclusive OR-gates as configured in the DeTroye patent insofar as it does not use them. Instead, the present invention uses only adders, rather than adders that are configured together with exclusive OR-gates to act as either adders or subtracters.

In light of the foregoing, Applicants respectfully submit that the DeTroye patent does not disclose the presently claimed invention insofar as it uses conventional CAS cells, such as disclosed in the background section of the present application.

Attorney's Docket'No. 030682-103 Application No. 09/667,783 Page 3

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above-captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: December 12, 2003

By:

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